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Distributed Sources of Passive Intermodulation on Printed Lines£

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The sources of Passive Intermodulation (PIM) on matched uniform microstrip lines have been investigated. The results of PIM measurements and SEM analysis of the conductor traces fabricated on the PCB laminates coated by copper foils of different grades suggest that PIM sources on the printed transmission lines are of non-local nature being distributed along the signal path. Quality of the copper foil and roughness of its surface proved to critically affect PIM performance of the microstrip lines on the low loss PTFE based dielectric substrates.

Introduction

Intermodulation (IM) phenomenon, which manifests itself in generation of combinatorial frequency signals resulting from nonlinear mixing of two or more single frequency signals, has been known for many decades as the source of spurious electromagnetic emission. Nowadays, it remains a major limiting factor of digital communication systems' performance because of a strong debilitating effect of IM interference on the network operation [1]. The use of tightly grouped, high power microwave signals and sensitive receivers impose stringent requirements on the admissible level of IM distortions, e.g. 3rd order IM products below –153 dBc have been specified for 3G mobile communications. At this level, even conventional passive microwave components, such as printed transmission lines (especially PCB based) and connectors, may cause prohibitively high IM interference. Therefore *Passive Intermodulation* (PIM) has become the subject of growing concern in the wireless community.

Significant progress has been recently made in rectifying numerous PIM sources, refining the design and manufacturing practices and establishing pertinent measurement procedures. As the result of these efforts, sources of PIM generation at joints of dissimilar materials, connectors, and cable assemblies have been thoroughly investigated, better understood and documented in the technical literature. At the same time, it was also observed that the printed transmission lines at the path of power signals might substantially contribute to PIM generation in RF assemblies. The significance of the PIM issues dramatically increases in the context of the prevailing trend towards integrated RF front end architectures where radiating elements, antenna beamforming networks, power distribution and matching circuits are fabricated on a single dielectric substrate.

The leading manufacturers of PCB materials can now consistently achieve -155dBc level of reflected PIM products. However to date, the causes and nature of PIMs on printed lines are little understood. Unlike PIMs in joints, connectors and cable transitions, PIM phenomena in printed circuits are scantly addressed in the technical literature. The information on PIMs at planar lines is available only from the PCB manufacturers [2,3] and a handful of publications (cf. [4]) on location of PIM sources on printed circuits. An objective of this paper is to examine the technological factors and mechanisms responsible for PIM generation by the non-localized sources on uniform microstrip lines.

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Transmission and reflection PIM products on uniform microstrip lines

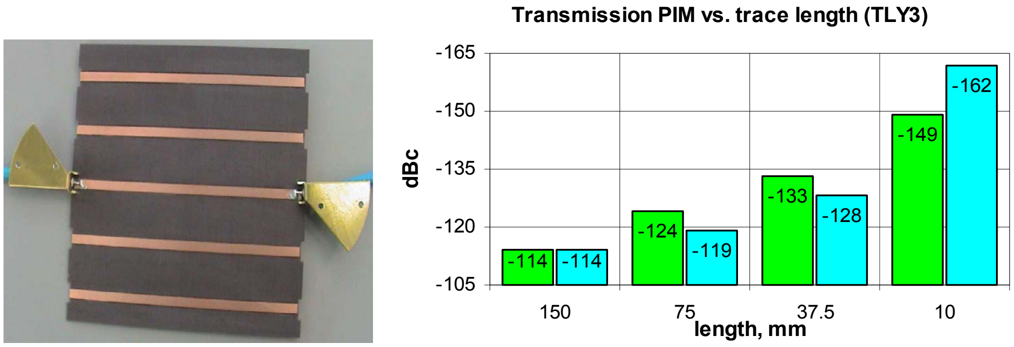
In order to identify the sources of PIM on printed transmission lines, a series of experiments have been carried out with the matched uniform microstrip lines fabricated on several PTFE based substrates (Fig. 1a, 2). The measurement results have shown certain distinctive features of PIM on the printed traces that fundamentally differentiate them from the PIM phenomena at spot joints and discontinuities of the signal path. In particular, Table 1 demonstrates that for all the tested materials, the 3rd order PIM level in transmission is higher than in reflection. Besides, a cumulative effect of PIM products in the transmitted signals can be seen in Fig. 1b for two samples of microstrip lines of several different lengths. These observations suggest that unlike connectors, spot contacts of dissimilar materials or line discontinuities, PIM sources on the printed traces are non-local being distributed along the signal path. The latter supposition is also supported by the fact that the level of PIM products in transmission is somewhat correlated with the insertion loss (cf. Table 1), viz. both PIM and losses simultaneously increase on the longer uniform microstrip traces, whilst PIM level in the reflected signals varies much less, normally remaining within the margins of the measurement uncertainty. Similar results have been earlier reported by NIST for coaxial cables [5].

Table 1. 3rd order PIM products (dBc) and Insertion Loss (dB) on 1m long 50 Ω microstrip lines at 1.8GHz

Material	MH0302ST	MX0302IM	SHEYI 2.45	TLC32	GML1000
PIM Reflection, dBc	-133	-124	-137	-127	-136
PIM Transmission, dBc	-113	-116	-	-113	-117
Insertion Loss, dB	-1.2	-1.5	-0.7	-1.2	-1.8

Printed conductors and PIM sources

To gain deeper insight into possible sources of PIM generation and accumulation on the printed lines, the PCB fabrication and processing factors have been re-examined. Investigations undertaken by the PCB manufacturers (see e.g. [2,3]) have exposed a number of technological aspects, which could cause PIM generation on the printed circuits. However copper foils have been identified as the primary contributor to the PIM performance of the printed transmission lines. The experiments with different grades of



(a) (b)

Fig. 1. 50 Ω microstrip lines on TLY3 (a); PIMs in transmitted signals at 1.8GHz (b).

copper and roughness of the foil surfaces adjoining PTFE laminate have exhibited strong correlation between the foil parameters and the PIM level on the uniform microstrip lines. In particular, the PIM measurements have consistently shown the lower level of PIM products on the foils with smoother surfaces. Apparently, roughness of the foil surface causes the material structural defects developing in the course of laminate manufacturing and etching the conductor patterns. The microscopic voids and impurities arising at the interfaces between the copper foil and dielectric substrate appear as inhomogeneities and nonlinear obstacles on the signal path.

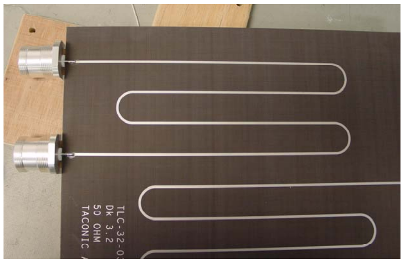


Fig. 2. Printed microstrip traces

In order to further explore impact of the foil properties on PIM generation on printed lines, the 50Ω microstrip meander lines of length 36” have been fabricated on the Taconic TLX-9-0620-7 base substrate (Dk=2.5) of size 9”×12”×0.63” (Fig. 2). The samples of the conductor traces were produced using three grades of copper foils which also had different surface roughness Rz (cf. Fig. 3):

A - standard electro-deposited copper (C1);
B - rolled annealed copper (R1); and
C - low-profile copper (CL1).

SEM micrographs in Fig. 3 display the fragments of open surfaces of the dielectric substrates and conductor edges of the etched microstrip traces for each sample. In the case **A**, the PTFE surface exhibits high porosity. Its open surface exposed by etching out the foil outside microstrip traces has the embossed topography inherited from the copper treatment. Residual unetched copper and other detritus are clearly visible inside the cavities adjacent to the etched trace “foot”. Conversely, PTFE surface of the sample **B** looks less deformed as compared to the sample **A**. However the conductor “wall” shows open crystalline (almost loose) copper structure exposed to oxidation. The PTFE surface of the specimen **C** has much smaller caverns than in the sample **A,** and there are less signs of debris at the trace “foot” too. The trace edge also looks more solid with rounded nodular appearance of copper that is a result of the CL1 foil manufacturing process.

PIM reflection tests were performed on the boards **A, B** and **C** using the Summitek tester and the kit SI1800. The measurement results of the 3rd order PIM products shown in Fig. 4 and summarised in Table 2 well correlate with the SEM analysis prediction. Indeed, the sample **C** with the higher quality of conductor traces and cleaner surrounding substrate

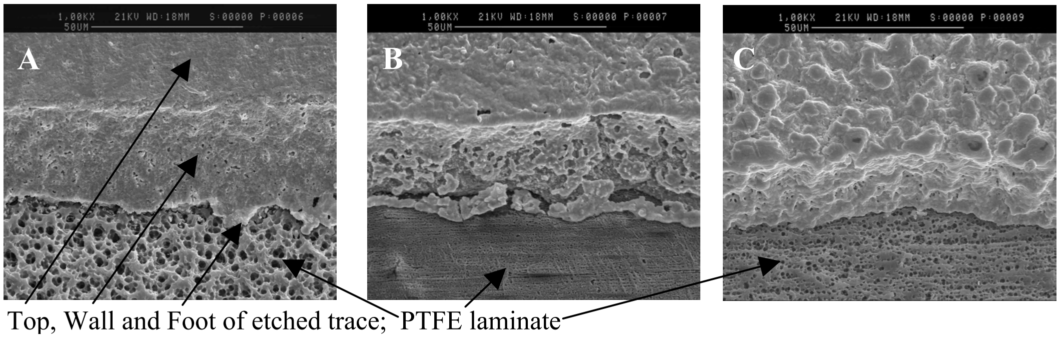


Fig. 3. SEM analysis of the etched traces on PTFE laminates with different grades of copper foils.
A: TLX-9-0620-7-CV1/CV1 (C1 - Standard Electro-deposited copper foil, Rz: 6μm to 9μm)
B: TLX-9-0620-7-R1/R1 (R1 – Rolled Annealed copper foil, Rz: 1μm to 2μm)
C: TLX-9-0620-7-CV1/CV1 (CL1 – Low Profile Electro-deposited copper foil, Rz: 2μm to 3μm)

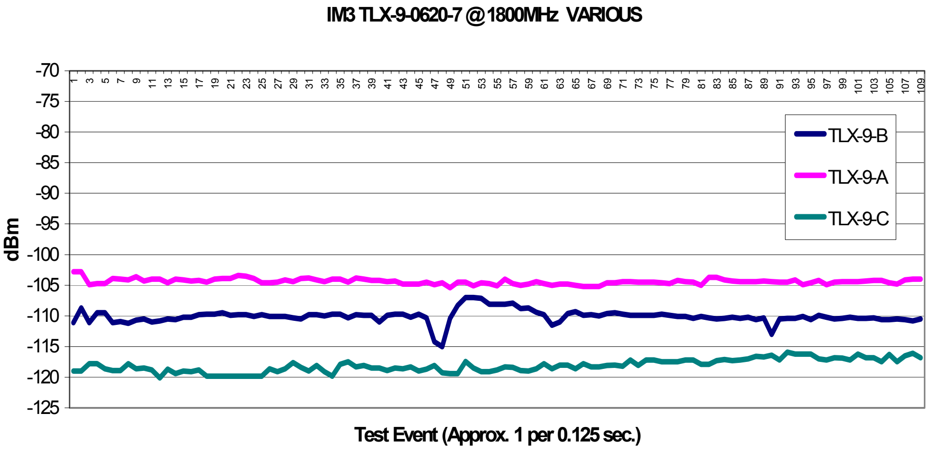


Fig. 4. Test results for 3rd order PIM products in samples **A**, **B** and **C**.

surface exhibits the lower PIM level than the samples **A** and **B**. The spots of incomplete copper etching and sites for debris, metallic or residual chemicals seen at the sample **A** proved to be particularly difficult to remove from the PTFE surfaces indented by the rough copper foil. These contaminants lying on the signal path and flaky conductor edges apparently act as the additional distributed microscopic PIM sources on the boards **A** and **B**. Alternatively, low-profile foil CL1 reduces the opportunity for incomplete etching and provides a “cleaner” and better defined trace wall and “foot”. Whilst R1 is also “low profile” foil, which was for some time recognized as a good material for low PIM laminates, on this occasion the trace wall and foot contain crystalline copper debris that have contributed to the higher PIM level.

Table 2. 3rd order PIM on TLX-9-0620 @ 1800MHz

Sample	Average IM3	Copper foil
TLX-9-**C**	-118 dBm [161 dBc]	CL1
TLX-9-**B**	-110 dBm [153 dBc]	R1
TLX-9-**A**	-104 dBm [148 dBc]	C1

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